REMARKS

At the time of the Office Action dated May 5, 2004, claims 1-20 were pending. Applicants acknowledge, with appreciation, the Examiner's allowance of claims 2-20. Only claim 1 stands rejected.

In this Amendment, new method claim 21 has been added, which was prepared based on claim 1. Care has been exercised to avoid the introduction of new matter.

Claim 1 has been rejected under 35 U.S.C. §102(b) as being anticipated by Lim et al.

In the statement of the rejection, the Examiner asserted that Lim et al. discloses a pipelined multi-stage analog-to-digital converter identically corresponding to what is claimed. This rejection is respectfully traversed.

It is well established that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicants submit that Lim et al. does not disclose an analog-to-digital conversion circuit specifically including "a group of correction values being preset for each value of an arbitrary digital signal outputted from said analog-to-digital converter," and "a correction value output circuit that outputs a corresponding correction value based on the digital signal outputted from said analog-to-digital converter," as recited

in claim 1 (emphasis added). In the forth full paragraph at page 2 of the Office Action, the Examiner asserted that "The Lim et al circuit includes a correction value output circuit (RAM 53) that stores preset correction values and a correction circuit (40, 60) that corrects the digital signal by way of operation based on the correction value output from the correction value circuit. However, Applicants respectfully disagree with the Examiner's position for the reasons set forth below.

In the claimed invention, an analog input signal is converted to a digital signal for output by an analog-to-digital converter. Based on the digital signal output from the analog-to-digital converter, a corresponding correction value is output from a correction value output circuit. The digital signal is corrected by way of operation by a correction circuit based on the correction value output from the correction value output circuit.

Applicants stress that the claimed invention has preset correction values including values corresponding to an arbitrary digital signal outputted from the analog-to-digital converter, and a correction value corresponding to a digital signal obtained from the analog-to-digital converter is selected from the group of correction value by the correction value output circuit. Therefore, errors that may occur in an analog-to-digital conversion can be reduced. This configuration can further eliminate any multiplier, thus reducing a circuit scale.

Lim et al. discloses in column 6, lines 13-30 that first-stage code errors are measured and quantized through latter stages and digital correction logic circuit 40. These errors are measured a predetermined number of times, averaged by an averaging logic circuit 52, and finally stored in a RAM 53. The errors stored in RAM 53 are then subtracted by a subtractor 60 from a 13-bit raw output code which is not calibrated but is corrected. The

least significant bit (LSB) is discarded to reduce truncation errors caused by digital processing, to result in a 12-bit linear output code.

As mentioned above, the reference discloses that the measured and quantized errors are stored in RAM 53, and subtracted from the 13-bit raw output code. However, Applicants submits that such description does not indicate the claimed preset correction values including values corresponding to an arbitrary digital signal outputted from the analog-to-digital converter, and a correction value corresponding to a digital signal obtained from the analog-to-digital converter is selected from the group of correction value by the correction value output circuit. Lim's measured and quantized errors in RAM 53 does not include values corresponding to an arbitrary digital signal outputted from the analog-to-digital converter, and no selection operation is carried out. Accordingly, Lim et al. does not disclose the "group of correction values" and "correction value output circuit," recited in claim 1.

The above-described fundamental differences between the claimed invention and Lim et al. undermine the factual determination that Lim et al. identically describes the claimed invention within the meaning 35 U.S.C. §102. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicants, therefore, respectfully submit that the imposed rejection of claim 1 under 35 U.S.C. §102(b) for lack of novelty as evidenced by Lim et al. is not factually viable and, hence, solicit withdrawal thereof.

Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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